SMARTLOGIC

Intel IP Catalog Flow

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V 1.4

Intel IP Catalog Flow

This AppNote describes how to use the IP catalog flow for all supported Intel FPGA devices

- How to generate the IP Core
- make specific parameter settings so that the generated IP runs with the Smartlogic core
- How to activate MSI and MSI-X interrupts (only available in the HCC version of the Smartlogic IP core)

Database preparation

In order to use the IP catalog flow it is necessary to reference to the correct files in the IP Database

- Make sure to use pcie_core_connection_ipi.vhd instead of pcie_core_connection.vhd, if you are not working in multifunction mode
- In case you work with multi-function, you have to to include pcie_core_connection_mf.vhd in the QSF file
- In case you migrate from the old flow to the new IP catalog flow, you have to delete the direct references to the Intel HIP related files. By adding the HIP IP core from the IP catalog, these files will be added automatically again in the background via the .ip / .qip files.
- A demo project is available that works as an example

For Cyclone V FPGAs two IP catalog cores have to be generated and added to the design:

1. The Transceiver Reconfiguration Controller Intel FPGA IP core with the IP variation filename „transceiver_reconfig.v“
2. The „Cyclone V Hard IP for PCI Express Intel FPGA“ IP core with the IP variation filename „intel_c5_pcie2.v“

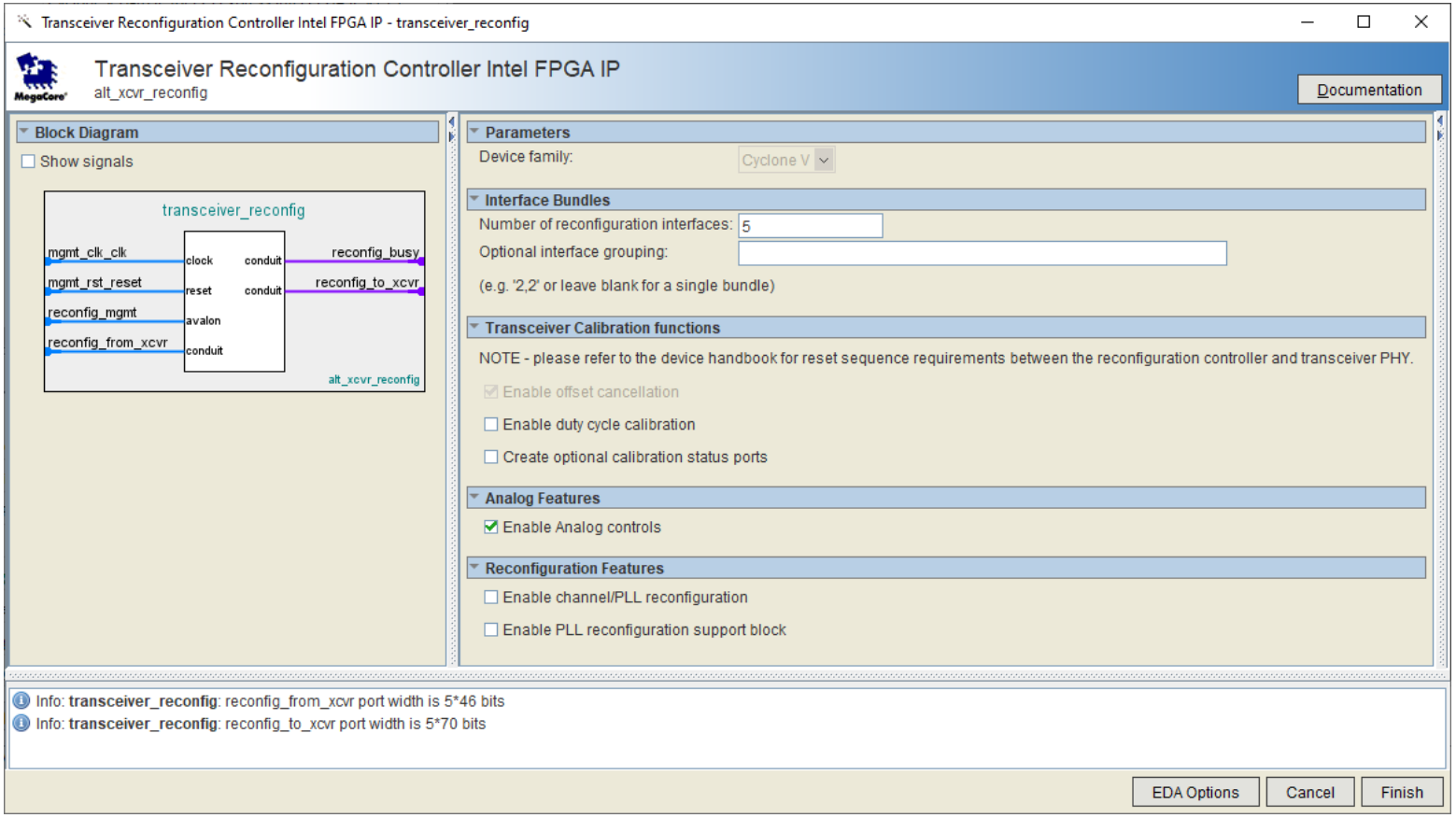
Select those IPs in the IP catalog and prepare them for configuration by double clicking.

Make sure that your project contains the following flow specific files:

• The file „pcie_core_connection_ipi.vhd“ has to be added to the project instead of pcie_core_connection.vhd in non multi function mode and pcie_core_connection_mf.vhd in multi function mode.

• The IP Core wrapper File „altera_a5_c5_pcie2_wrapper.v“ has to be added to the project instead of the file „altera_c5_pcie2.sv“

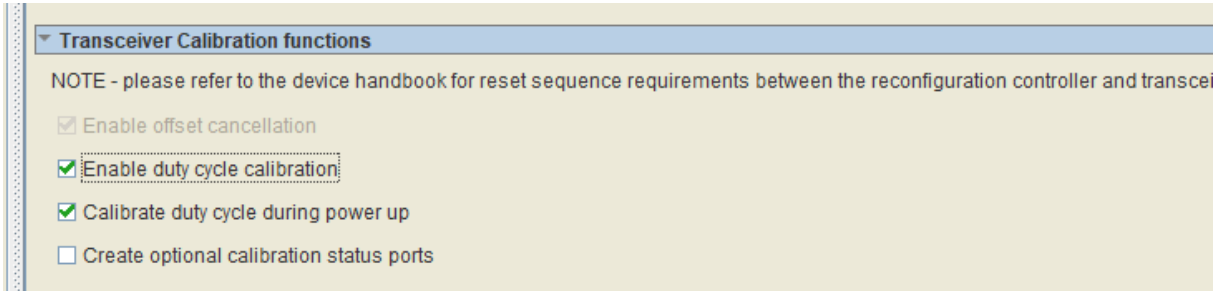
GUI of the Transceiver Reconfiguration Controller



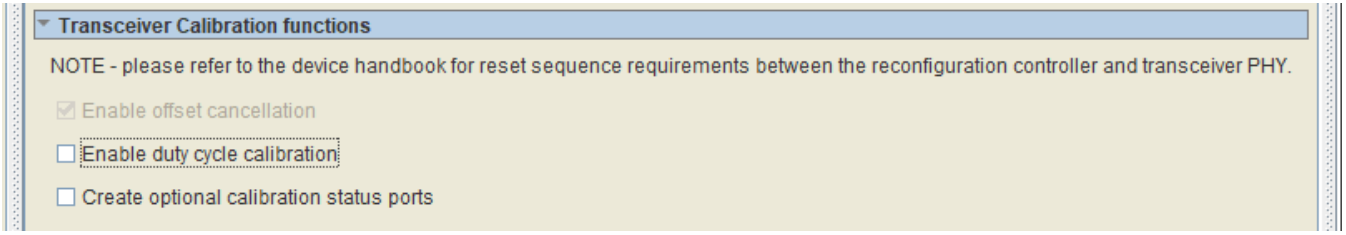
Special care has to be taken regarding the number of reconfiguration interfaces and the duty cycle correction. The next two slides show how to configure them correctly.

Duty cycle correction : Working around a Quartus Prime GUI Problem

First check „Enable duty cycle calibration“ and the GUI should look like this:



Now deselect Enable duty cycle calibration, while leaving „Calibrate duty cycle during power up“ checked and the GUI looks like this :



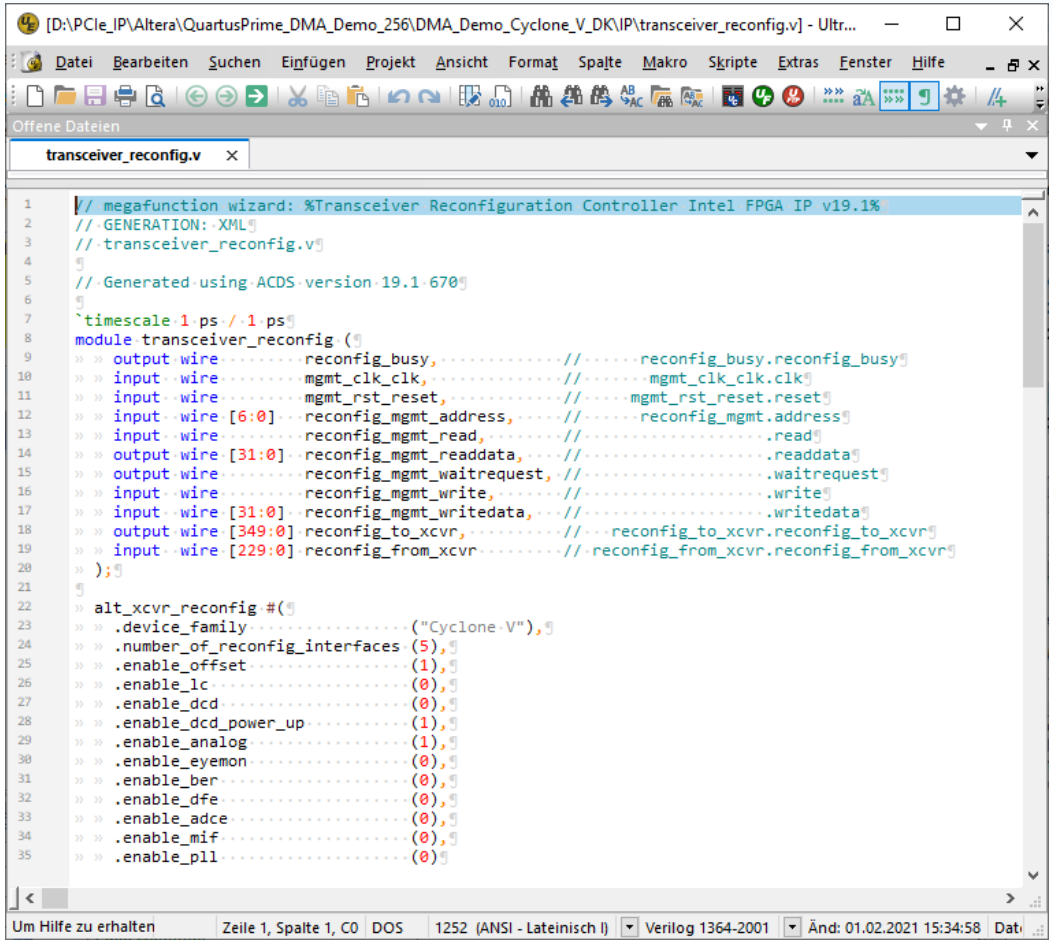
Although it seems, that no duty cycle calibration is selected, the „Calibrate duty cycle during power up“ is still active. This is the correct setting.

Cyclone V – Number of reconfiguration interfaces

The number of reconfiguration interfaces has to be entered according to the following table:

PCIe Linkwidth	Number of reconfiguration interfaces
X1	2
X2	3
X4	5

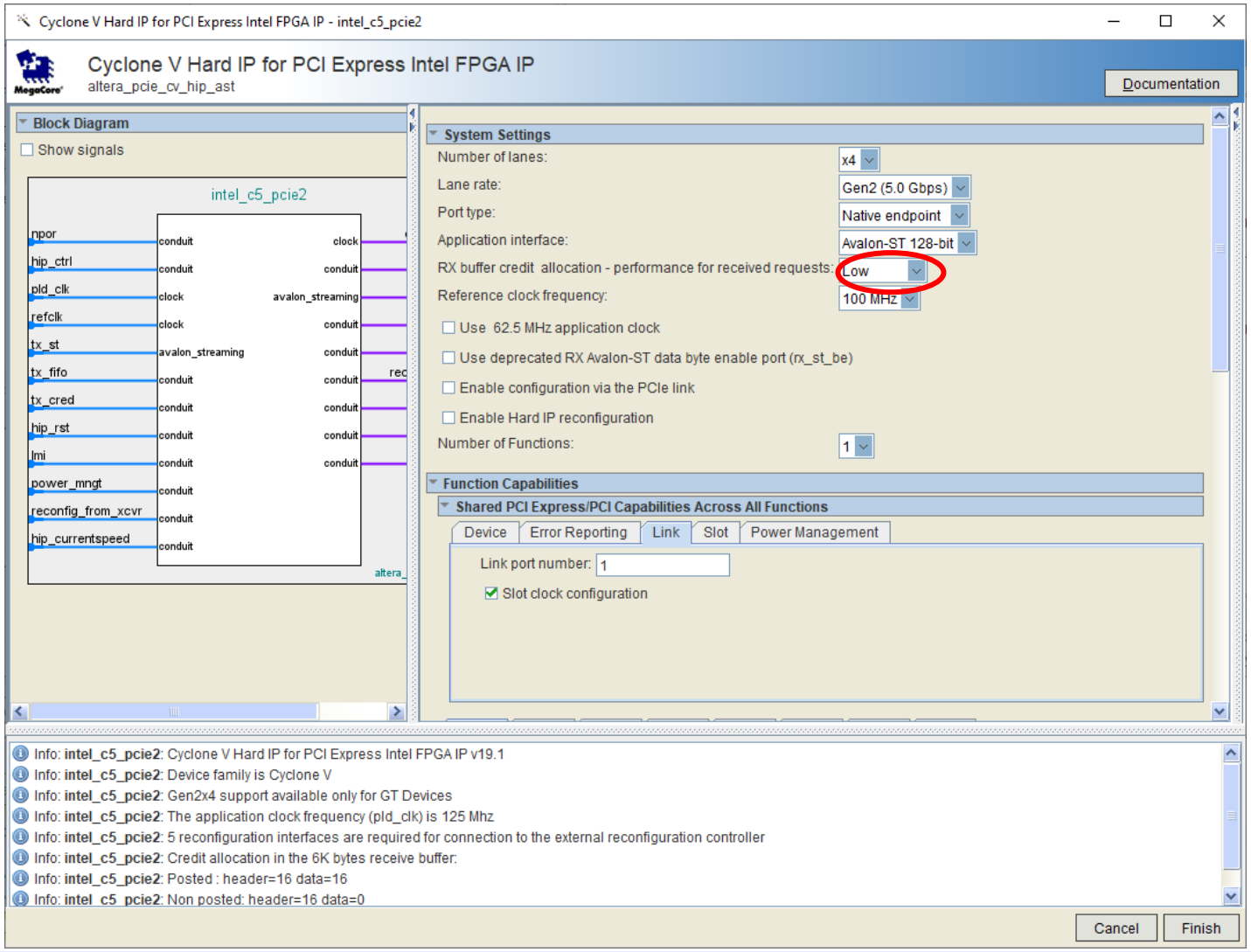
Cyclone V – Transceiver Reconfiguration Controller



After you have generated the Transceiver Reconfiguration Controller, open the generated file „transceiver_reconfig.v“ with a text editor. The parameter settings of alt_xcvr_reconfig .enable_dcd must be 0 and .enable_dcd_power_up, .enable_offset and .enable_analog must be 1. If they have a different setting, repeat the configuration process for the IP.

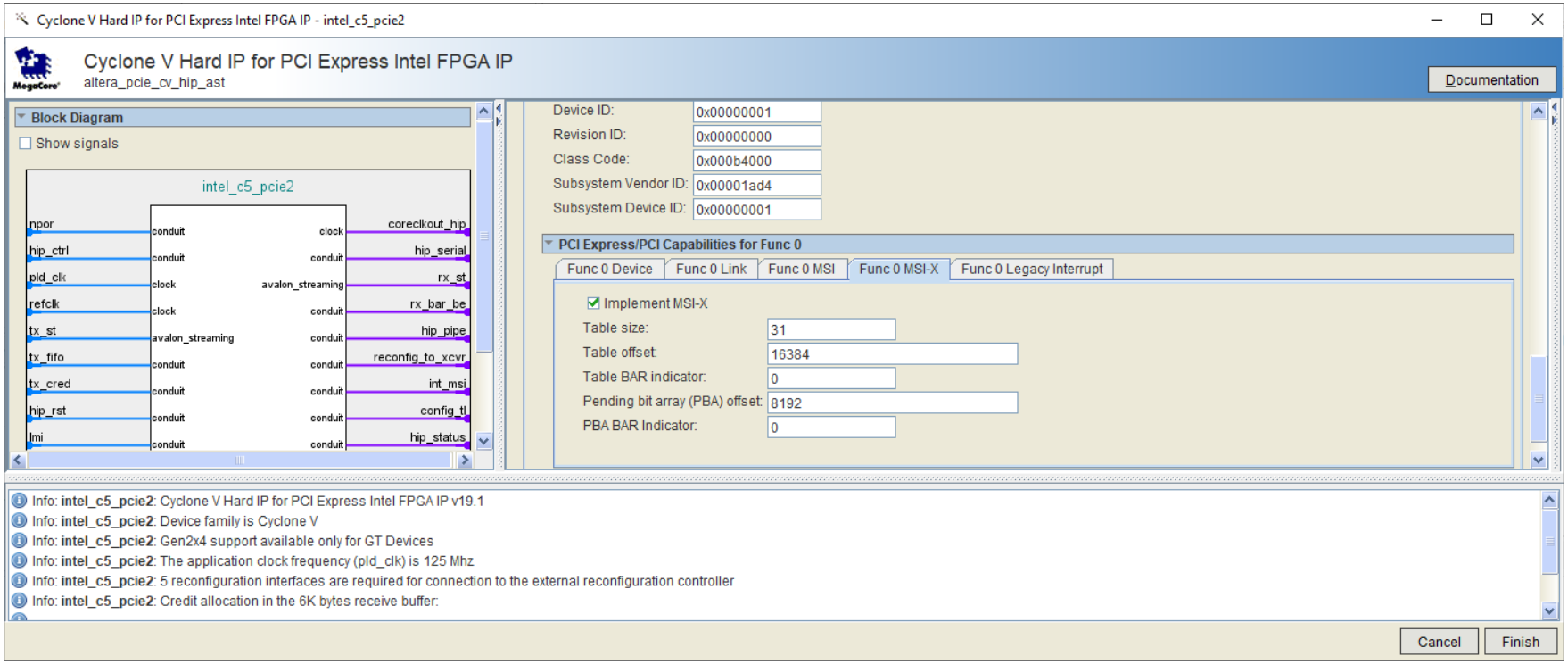
Cyclone V – Configuring the HIP

GUI of the Cyclone V HIP:



Cyclone V – Configuring MSI-X (only available for the HCC core)

GUI of the Cyclone V HIP : Example how to activate 32 MSI-X interrupts :



Currently only 32 MSI-X interrupts are supported, please do not try to enter other values.

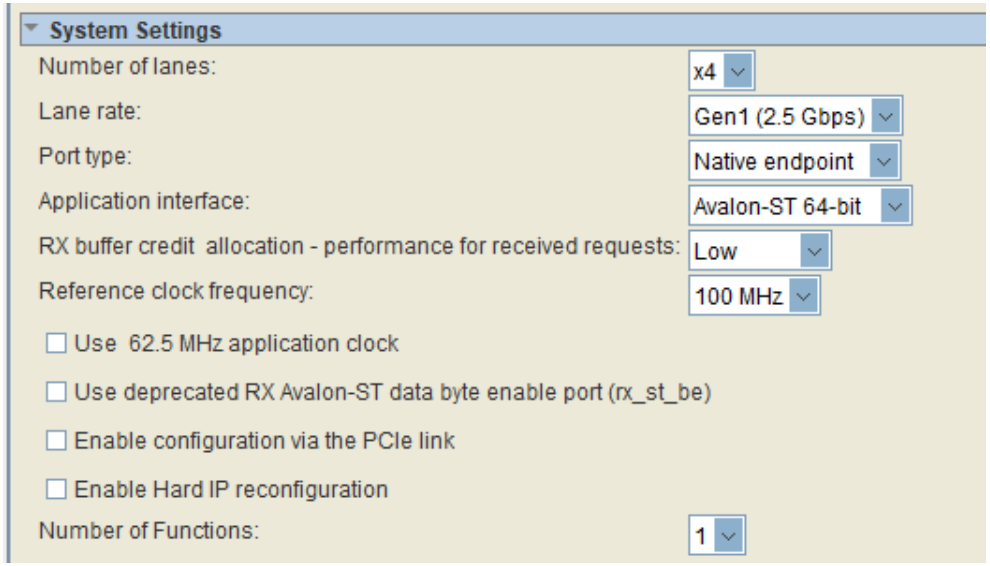
Also make sure to set the generic/parameter use_msix_g to 1 !

Cyclone V – working around a HIP GUI Error

It has been observed for Cyclone V, that the GUI parameters might not be transferred correctly to the IP‘s HDL parameter section during the IP generation process of Quartus. This problem happens especially when the link speed is changed form Gen2 to Gen1. In this case the GUI looks right, but the 62.5 MHz option is activated in error. This results in an illegal PCIe HIP configuration and the FPGA design does not communicate correctly via PCIe and causes a system crash.

A clear indication that your design is affected is when Quartus reports warning message #332056.

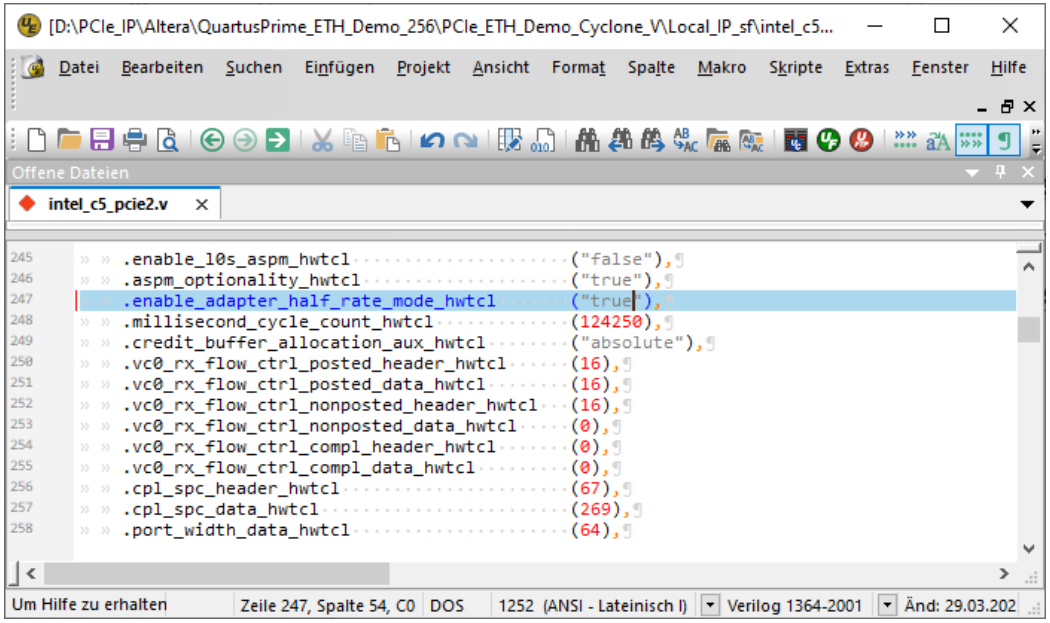
Example:



Although „use 62.5 MHz application clock“ is unchecked, the generated IP might have this option turned on.

Cyclone V – working around a HIP GUI Error

In order to check, if your design is affected, open the generated file intel_c5_pcie2.v and search for the parameter .enable_adapter_half_rate_mode_hwtcl:



If this parameter is set to „true“ and you are not operating in G2-X4 mode, your design is affected.

In this case you have to set all 4 checkboxes in the „System Settings“ Tab (see previous page) and then clear them all and re-generate the IP again. Do not change the verilog file as it will be overwritten when you change other parameters. After re-generating the file, re-check if the setting of enable_adapter_half_rate_mode_hwtcl is now correct.

Cyclone V – working around a HIP GUI Error

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Summary of the Quartus GUI Error:

- The GUI error seems to affect all IP cores
- Problem is, that the GUI representation of the checkboxes seems not to be in sync with the real parameter values
- This problem leads to illegal designs and even system crashes
- It has been observed in QuartusPrime Lite 19.1 and might occur also in newer versions
- Most likely it affects not only Cyclone V but also all other FPGA design families

Cyclone V – Configuring the HIP

Important when you configure the Cyclone V HIP core:

- Never check „Use 62.5 MHz application clock“. The Smartlogic IP will not work with this setting
- Never check „use rx_st_be“
- Set the RX Buffer credit allocation to „Low“ when the FPGA uses DMA Read. In all other cases, set this to „Balanced“
- You may turn on „Enable configuration via the PCIe link“ also known as CVP
If you turn on CVP make sure, that the PCIe 100 MHz reference clock is connected to sys_clk_ip of the Smartlogic IP core and that a free running 125 MHz clock is connected to sys_clk_in of the Smartlogic IP core. If you do not work with CVP, connect the 100 MHz clock to both sys_clk_ip and sys_clk_in
- Check „slot clock configuration“, if you are operating with a common reference clock between root complex and FPGA endpoint
- If you are running in Gen2-X4 mode, make sure to set the Application interface to Avalon-ST 128-Bit. In all other cases use the 64-Bit version
- Set the Device Identification Registers and the PCI Express Capabilities for Func 0 according to your needs
- You may configure additional PCIe functions in case you have a multi-function license

A demo design, where the Cyclone V IPs are correctly setup, is available from Smartlogic.

Make sure to configure the following parameters of the Smartlogic IP core in the same way as you entered them into the HIP GUI:

pcie_ep_config_pkg.vhd

Parameter	Comment
PCIe_synth_Core_Type_c	„CV“
Enable_SLOT_CLOCK_C PCIE_MSI_CAP_MULTIMSGCAP_C PCIe_BAR<x>_C PCIe_CLASS_CODE_C PCIe_VEN_ID_C PCIe_DEV_ID_C PCIe_SUBSYS_VEN_ID_C PCIe_SUBSYS_DEV_ID_C PCIe_link_cap_max_link_speed_c PCIe_link_cap_max_link_width_c	Set these constants in the same way as you entered them in the GUI.

Cyclone 5 – Selecting the correct Avalon-ST bitwidth

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The Avalon ST data bitwidth has to be entered according to the following table:

PCIe Linkspeed / Linkwidth	Avalon ST bitwidth
G2-X4	128
G1-X8	128
All other link width / link speed combinations	64

For Arria 10 FPGAs one IP catalog core has to be generated and added to the design:

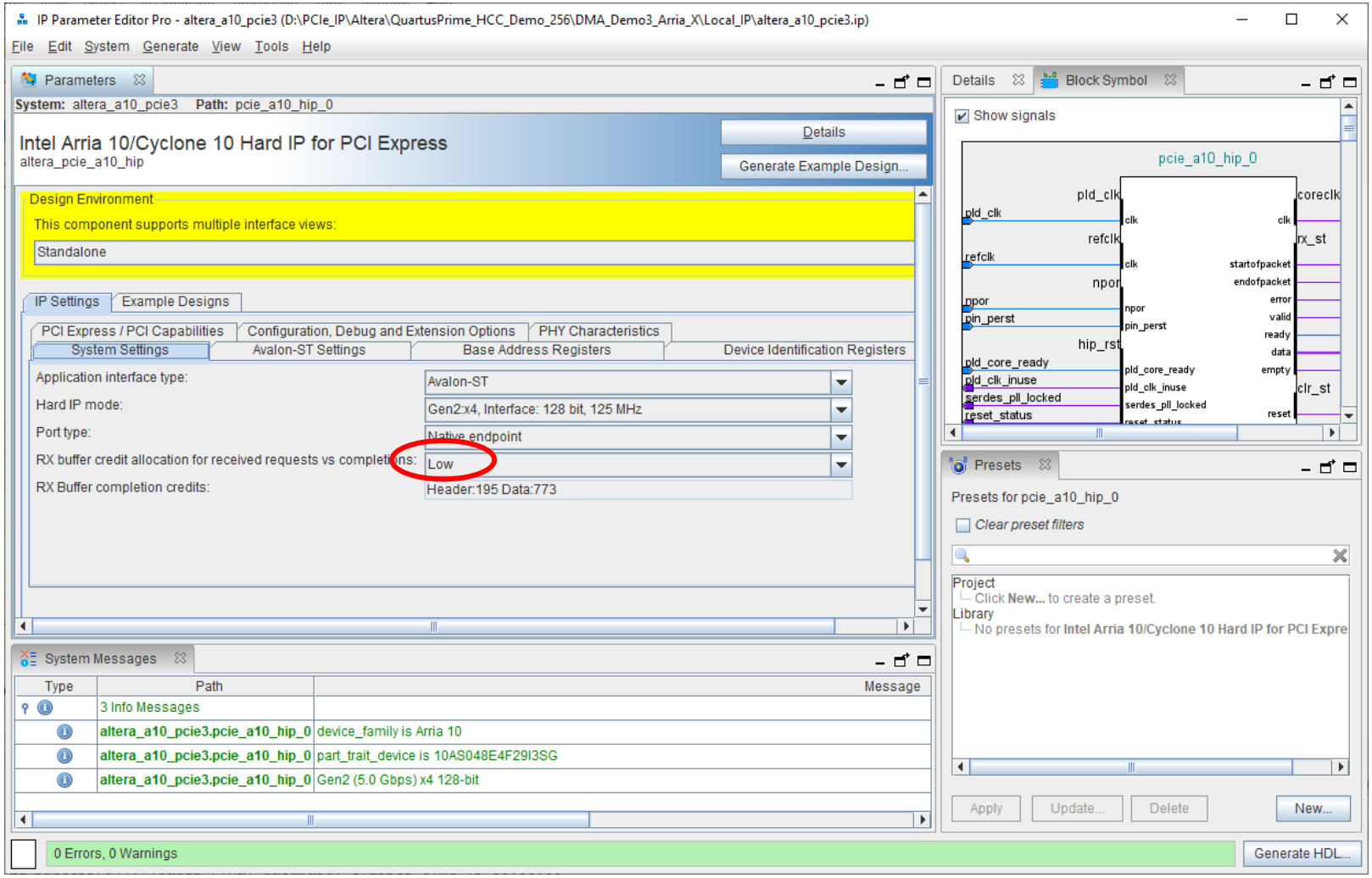
1. The „Arria 10 Hard IP for PCI Express“ IP core with the IP variation filename „altera_a10_pcie3.v“

Make sure that your project contains the following flow specific files:

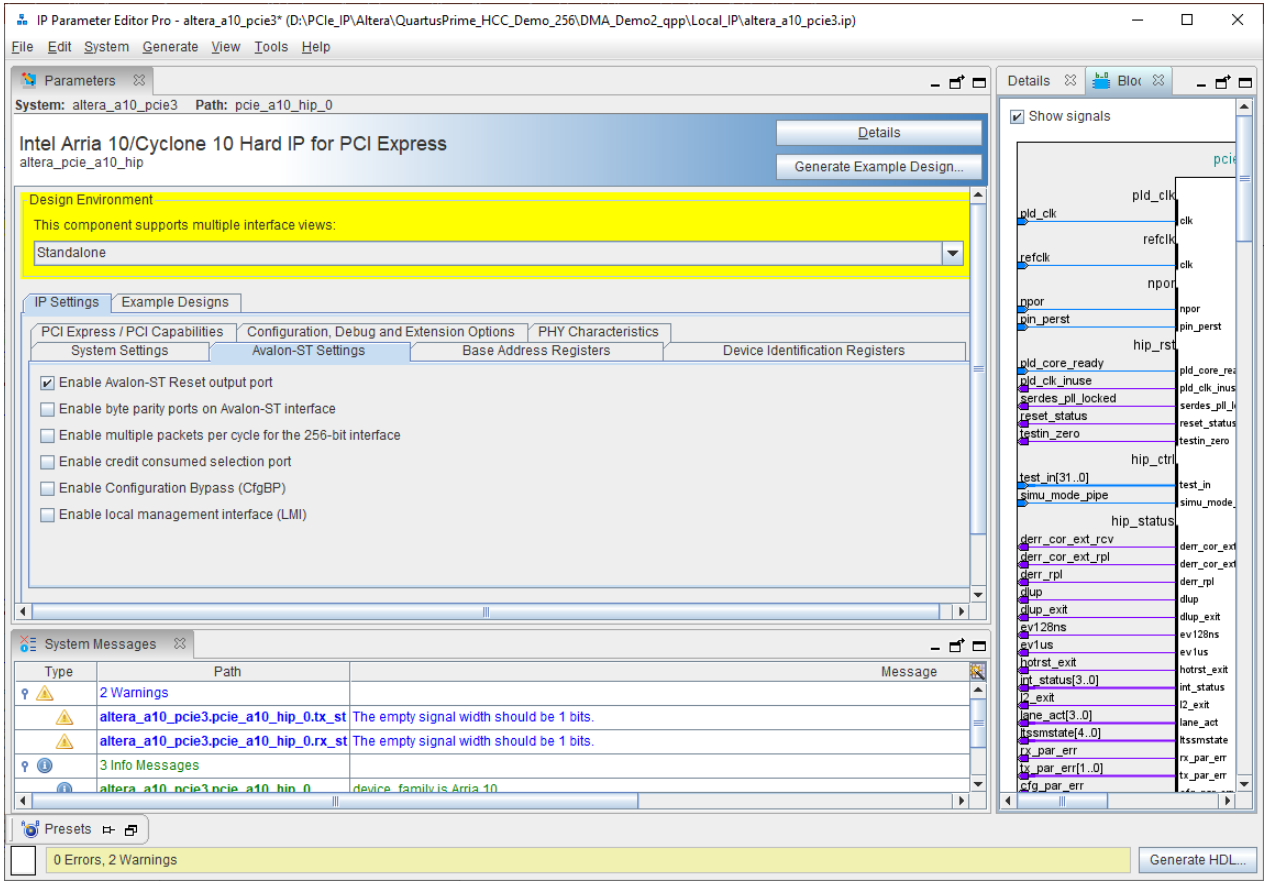
- The file „pcie_core_connection_ipi.vhd“ has to be added to the project instead of pcie_core_connection.vhd. Note that PCIe multi-function is not supported from the PCIe HIP for Arria 10.
- The IP Core wrapper File „altera_a10_pcie3_wrapper.v“ has to be added to the project

Arria 10 – Configuring the HIP

GUI of the Arria 10 HIP:



GUI of the Arria 10 HIP:



Enable only the Avalon-ST Reset output port. Never turn on „Enable multipackets per cycle for the 256-Bit Interface“

Arria 10 – Configuring the HIP

Important when you configure the Arria 10 HIP core:

- Set the RX Buffer credit allocation to „Low“ when the FPGA uses DMA Read. In all other cases, set this to „Balanced“
- You may turn on „Enable configuration via the PCIe link“ also known as CVP

If you turn on CVP make sure, that the PCIe 100 MHz reference clock is connected to sys_clk_ip of the Smartlogic IP core and that a free running 125 MHz clock is connected to sys_clk_in of the Smartlogic IP core. If you do not work with CVP, connect the 100 MHz clock to both sys_clk_ip and sys_clk_in

- For Signal Integrity measurements, you may turn on ADME to use the transceiver toolkit
- Check „slot clock configuration“, if you are operating with a common reference clock between root complex and FPGA endpoint
- Set the Device „Identification Registers“ and the „Base Address Registers“ according to your needs
- Choose „maximum payload size“ according to the capabilities of your root complex
- The Arria 10 PCIe HardIP does not support PCIe multi-function

A demo design, where the Arria 10 HIP is correctly setup is available from Smartlogic.

Make sure to configure the following parameters of the Smartlogic IP core in the same way as you entered them into the HIP GUI:

pcie_ep_config_pkg.vhd

Parameter	Comment
PCIe_synth_Core_Type_c	„AX“
Enable_SLOT_CLOCK_C PCIE_MSI_CAP_MULTIMSGCAP_C PCIe_BAR<x>_C PCIe_CLASS_CODE_C PCIe_VEN_ID_C PCIe_DEV_ID_C PCIe_SUBSYS_VEN_ID_C PCIe_SUBSYS_DEV_ID_C PCIe_link_cap_max_link_speed_c PCIe_link_cap_max_link_width_c	Set these constants in the same way as you entered them in the GUI.

Arria 10 – Selecting the correct Avalon-ST bitwidth

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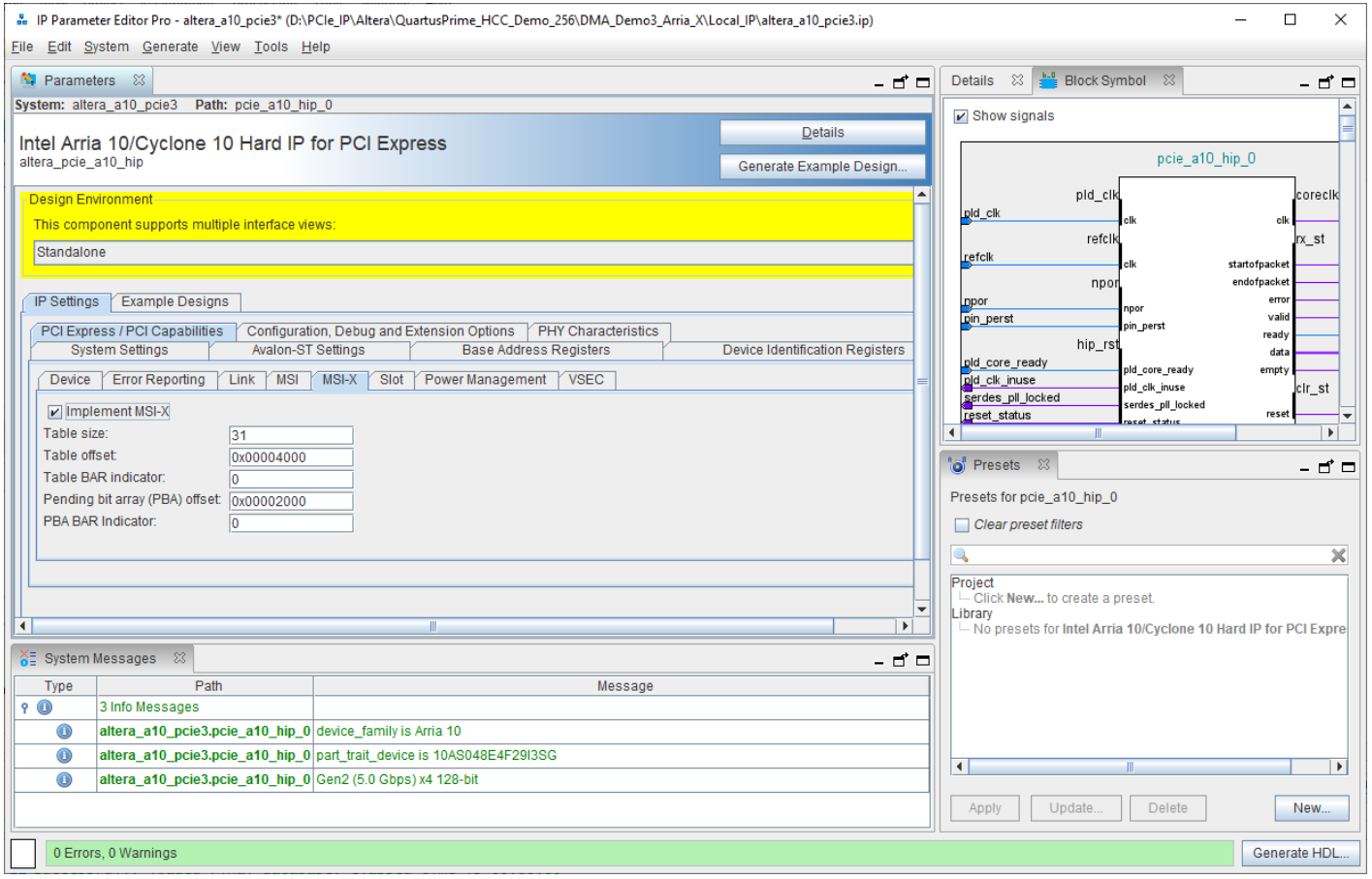
The Avalon ST data bitwidth has to be entered according to the following table:

PCIe link speed / link width	Avalon ST bit width
G3-X8, G3-X4, G2-X8	256
G1-X8, G2-X4, G3-X2	128
G1-X1, G1-X2, G1-X4, G2-X1, G2-X2, G3-X1	64

Arria 10 – Configuring MSI-X (only available for the HCC core)

GUI of the Arria 10 HIP : Example how to activate 32 MSI-X interrupts :



Currently only 32 MSI-X interrupts are supported, please do not try to enter other values.

Also make sure to set the generic/parameter use_msix_g to 1 !

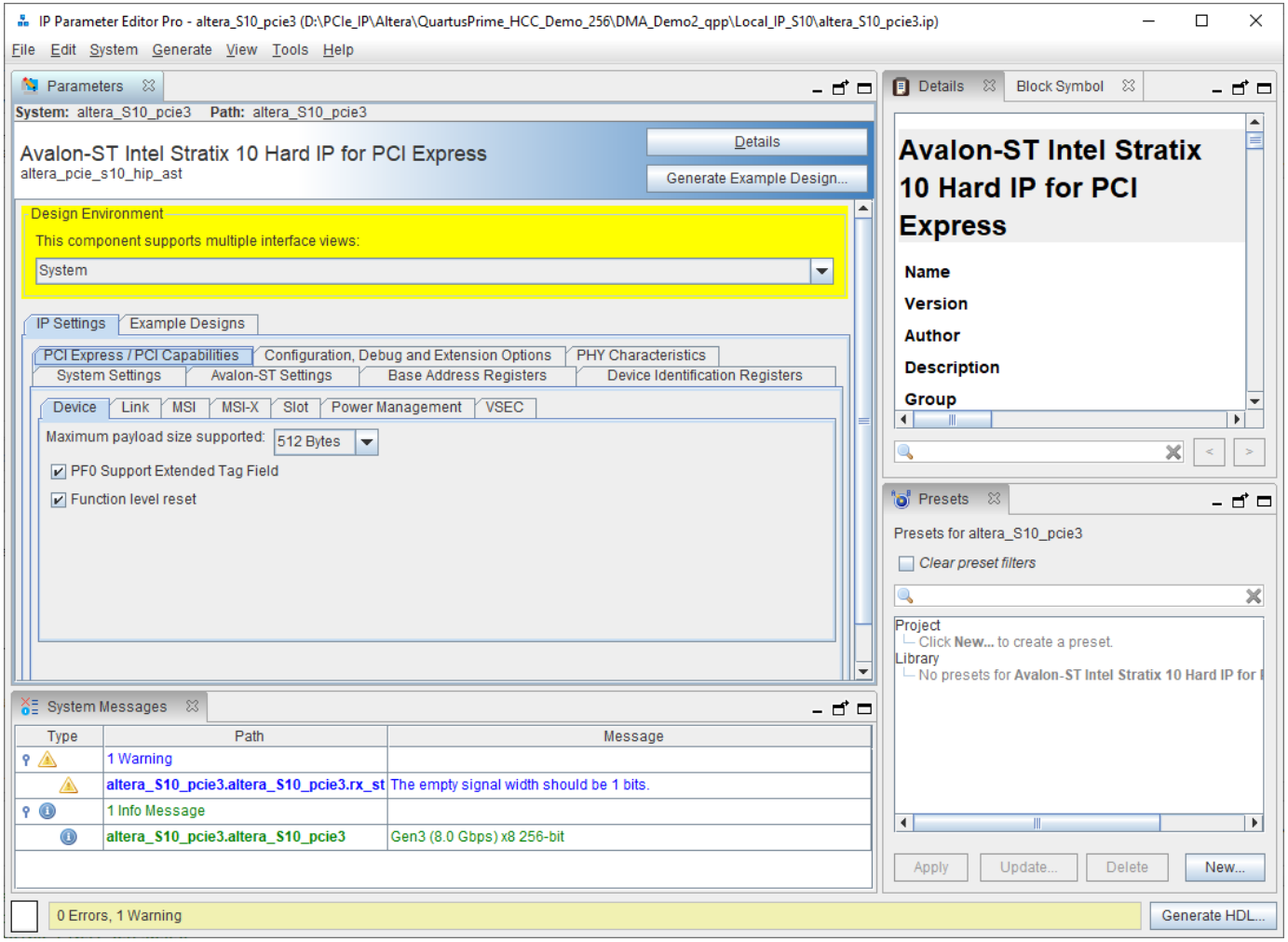
For Stratix 10 FPGAs one IP catalog core has to be generated and added to the design:

1. The „Avalon-ST Intel Stratix 10 Hard IP for PCI Express“ IP core with the IP variation filename „altera_S10_pcie3.v“

Make sure that your project contains the following flow specific files:

- The file „pcie_core_connection_ipi.vhd“ has to be added to the project instead of pcie_core_connection.vhd
- The IP Core wrapper File „altera_s10_pcie3_wrapper.v“ has to be added to the project

GUI of the Stratix 10 HIP:



Important when you configure the Stratix 10 HIP core:

- You may turn on „Enable configuration via the PCIe link“ also known as CVP

If you turn on CVP make sure, that the PCIe 100 MHz reference clock is connected to sys_clk_ip of the Smartlogic IP core and that a free running 125 MHz clock is connected to sys_clk_in of the Smartlogic IP core. If you do not work with CVP, connect the 100 MHz clock to both sys_clk_ip and sys_clk_in

- For Signal Integrity measurements, you may turn on ADME to use the transceiver toolkit
- Check „slot clock configuration“, if you are operating with a common reference clock between root complex and FPGA endpoint
- Set the Device „Identification Registers“ and the „Base Address Registers“ according to your needs
- Choose „maximum payload size“ according to the capabilities of your root complex
- In case you are working with DMA Read you can check the „PF0 Support Extended Tag Field“ to improve performance. However this uses more BRAM resources
- multifunction is only supported for Stratix H-Tile devices

A Demodesign, where the Stratix 10 HIP is correctly setup is available from Smartlogic as a reference.

Stratix 10 – Selecting the correct Avalon-ST bit width

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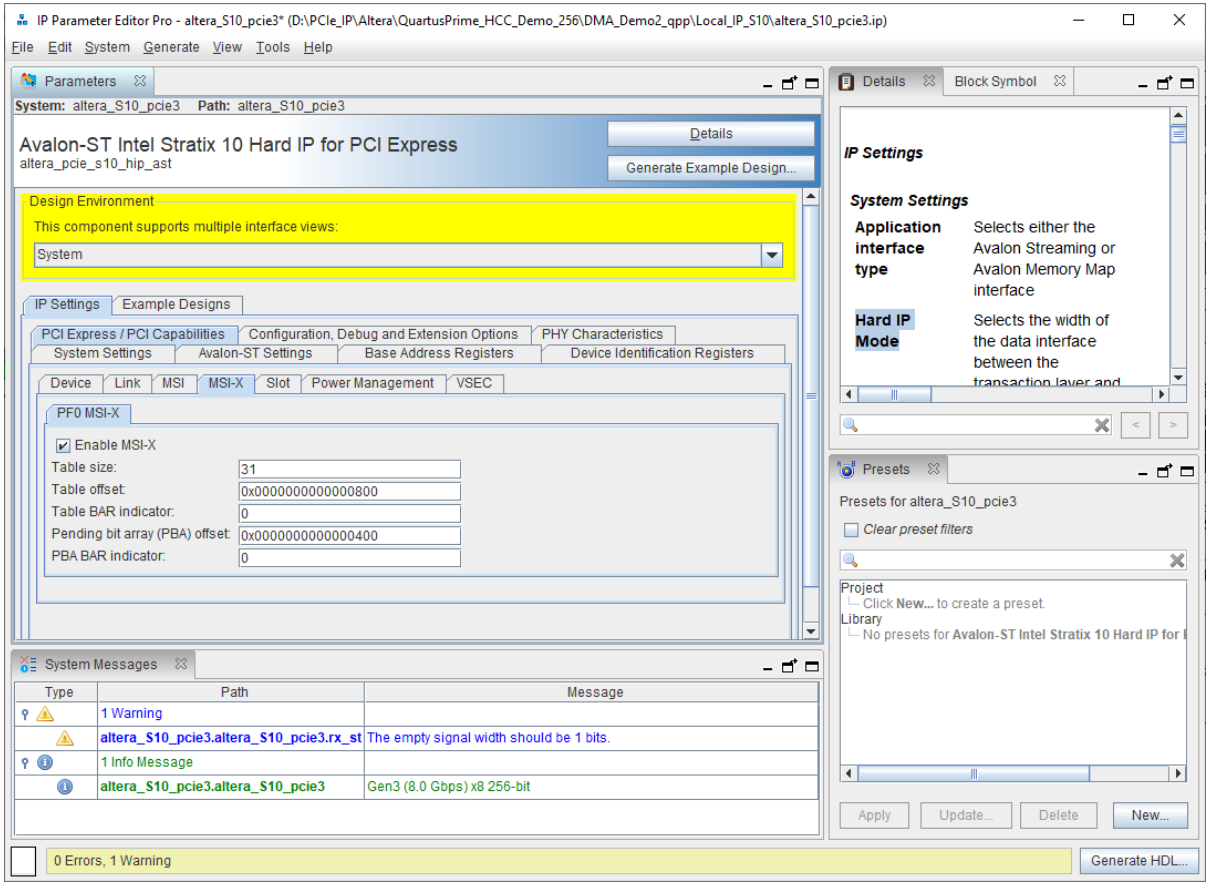
The Avalon ST data bit width has to be entered according to the following table:

PCIe Linkspeed / Linkwidth	Avalon ST bitwidth
G3-X8, G3-X4, G2-X8, G2-X16	256
G1-X8, G2-X4, G3-X2	128
G1-X1, G1-X2, G1-X4, G2-X1, G2-X2, G3-X1	64

Stratix 10 – Configuring MSI-X (only available for the HCC core)

GUI of the Stratix 10 HIP : Example how to activate 32 MSI-X interrupts :



Currently only 32 MSI-X interrupts are supported, please do not try to enter other values.

Also make sure to set the generic/parameter use_msix_g to 1 !

Make sure to configure the following parameters of the Smartlogic IP core in the same way as you entered them into the HIP GUI:

pcie_ep_config_pkg.vhd

Parameter	Comment
PCIe_synth_Core_Type_c	„SX“
Enable_SLOT_CLOCK_C PCIE_MSI_CAP_MULTIMSGCAP_C PCIe_BAR<x>_C PCIe_CLASS_CODE_C PCIe_VEN_ID_C PCIe_DEV_ID_C PCIe_SUBSYS_VEN_ID_C PCIe_SUBSYS_DEV_ID_C PCIe_link_cap_max_link_speed_c PCIe_link_cap_max_link_width_c	Set these constants in the same way as you entered them in the GUI.