

## High Channel Count DMA IP Core for PCI-Express

### Product Overview

The High Channel Count DMA IP Core for PCI-Express is a powerful PCIe Endpoint with multiple industry standard AXI Interfaces. This IP addresses continuous streaming applications from up to 64 different datasources. Each channel is able to transmit data into a separate memory area. Up to 16 AXI Stream Masters read DMA Data from the Host and present it to the User Logic. Additional 8 AXI4 Masters are available to interface full AXI or AXI-Lite peripherals with the Host.

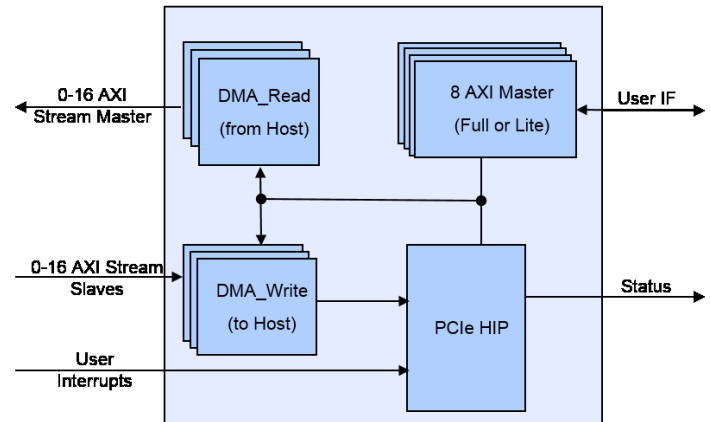
The Link Stability detector module measures the signal integrity of the PCI Express Link for lab or production tests to prevent shipments of faulty devices (Xilinx only).

This IP Core enables the developer to build complex PCI Express endpoints with no specific PCI Express Protocol Know How. The user only transmits/receives payload data and does not have to build valid PCI Express packets.

### IP-Features

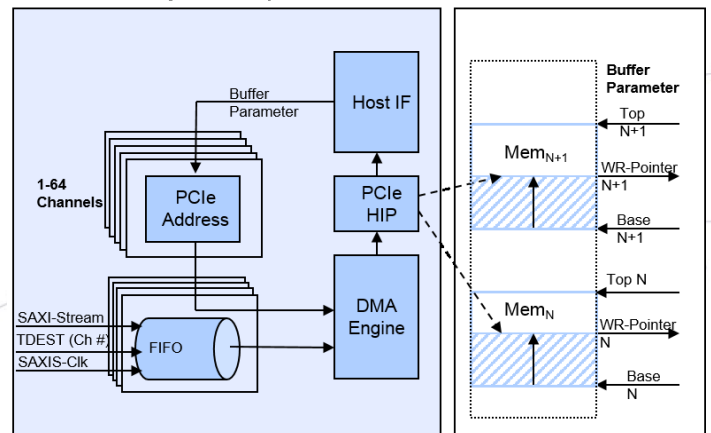
- Available for Xilinx or Intel (Altera) Devices
- User transmits / receives only user data without PCIe protocol knowledge
- AXI standard interfaces for easy integration
- All AXI Interfaces have adjustable Datawidth and separate clocking
- Supports up to 64 independent Host Buffers
- adjustable Priority Control
- Supports Scatter / Gather Memory with adjustable pagesize
- Supports linear contiguous Memory as Ringbuffers
- Memory Size up to 4 GByte per Streaming Channel
- Performance only limited by PCI-Express Bandwidth
- Based on Xilinx / Intel integrated PCI-Sig compliant PCIe Block (HIP)
- Link Speeds Gen1-3, Link Widths x1-x8

**High Channel Count DMA IP**



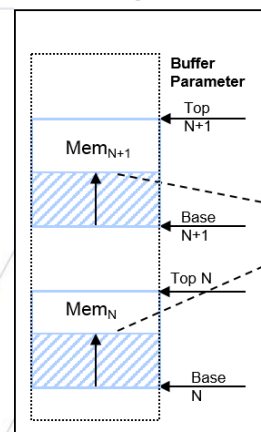
Block Diagram of the IP Core (simplified)

**FPGA to Host (DMA-Write)**

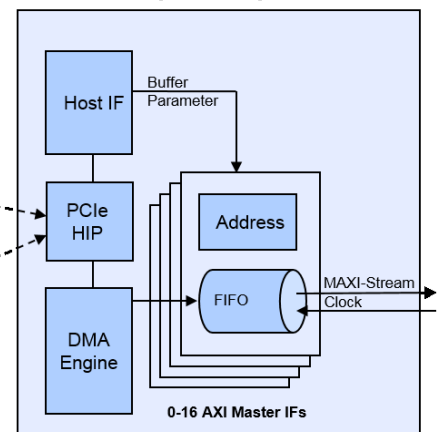


DMA Write Details

**Host Memory**



**Host to FPGA (DMA Read)**



DMA Read Details

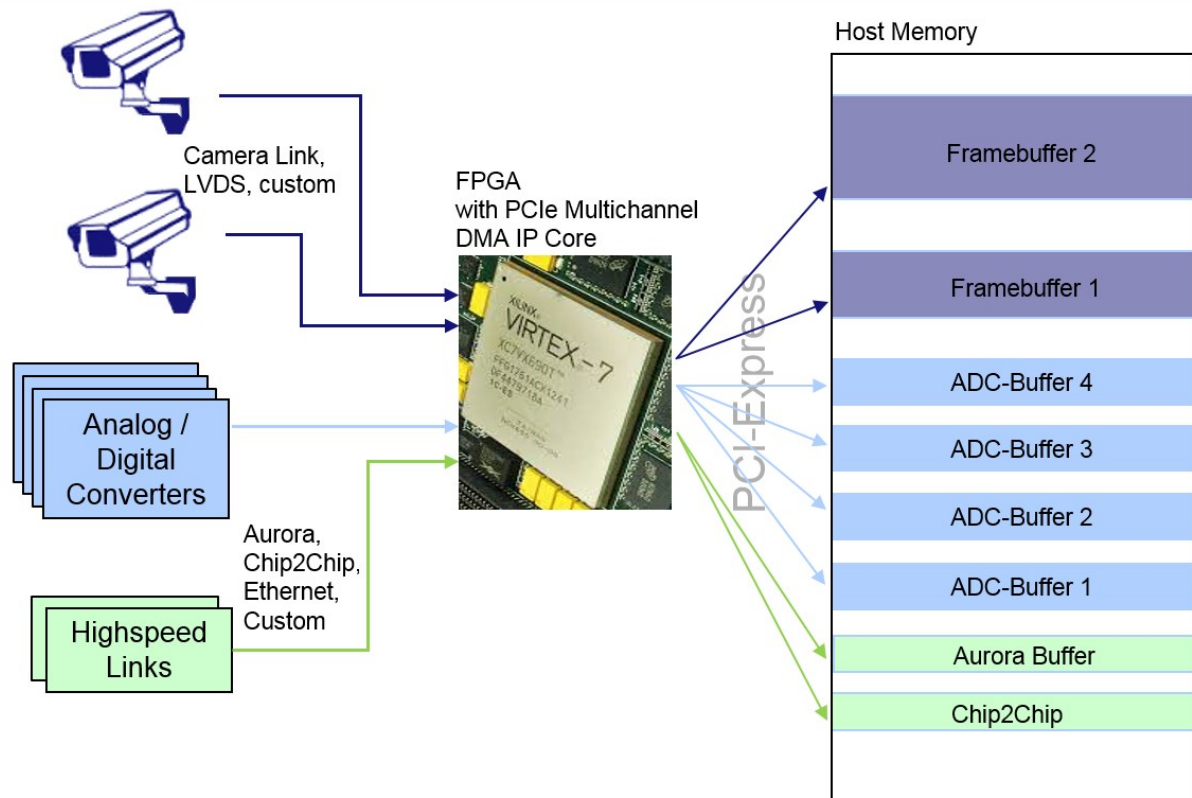
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## High Channel Count DMA IP Core for PCI-Express

### IP Application “Streaming”

Due to its generic architecture, the Multichannel DMA IP Core for PCI Express fits into many applications.

The following diagram shows the typical streaming application, where datastreams have to be sent ordered to the Host memory:



Typical streaming data sources are :

Video Cameras, Highspeed Analog-Digital-Converter Samples, Highspeed Links like Aurora, Ethernet or others.

Up to 64 independent streaming sources with a dedicated Target Buffer are supported.

Each data interface can operate at its own clock domain and its own datawidth (8, 16, 32, 64, 128 or 256 Bit).

The target can be either the Host Memory or any other PCI Express endpoint in the system.

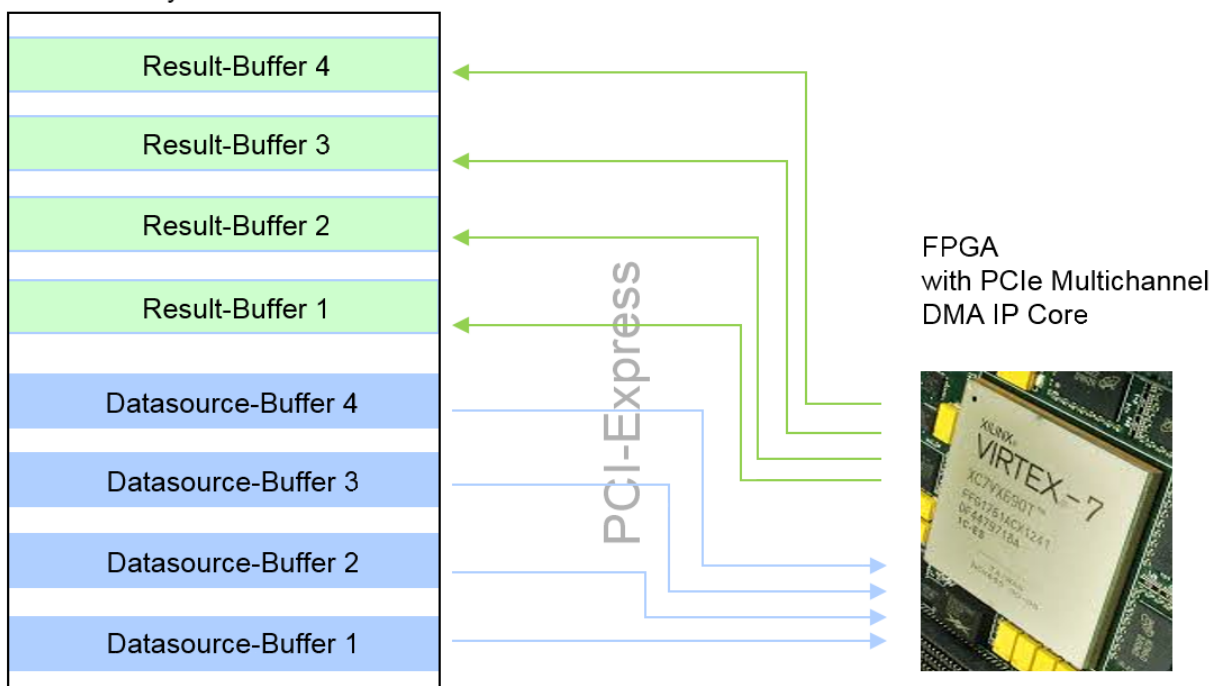
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### IP Application “Co-Processor”

Another well known application is the custom data Co-Processor within a FPGA. The data which has to be processed is either fetched via DMA Read Requests from the FPGA or served from the CPU or an other PCI Express endpoint. The processed results will be written back into separate memory buffers by using DMA Write Requests. Application examples are data encryption and Video Data processing.

Host Memory



### FPGA Resource Utilization

The following table lists different example configurations and the needed FPGA Resources:

FPGA Family	Configuration	FPGA-Resources <sup>(1)</sup>					
		LUTs	LUTR <sup>(2)</sup>	FFs	BRAM	PCIE	Misc
Artix 7 Kintex 7	64 bit Architecture, X4, Gen 1 32 DMA Write Channels, 1 Master, 0 Read Channels	5,583	235	7,377	9	1	1 MMCM
Artix 7 Kintex 7	64 bit Architecture, X4, Gen 1 32 DMA Write Channels, 1 Master, 8 Read Channels	9,068	463	10,112	25	1	1 MMCM
		ALMs		FFs	BRAM	PCIE	Misc
Arria 5							
Cyclone 5	256 bit Architecture, X4, Gen 2 32 DMA Write Channels, 1 Master, 8 Read Channels	9,555		15,757	95	1	6 PLL

(1) These numbers include the resources of the PCIe Hard-IP and the resources for the AXI Stream FIFOs for each configured channel.

(2) LUTR are distributed RAM Cells. For Xilinx FPGAs, the User can choose between BlockRAM or LUT RAM Implementation style.

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## High Channel Count DMA IP Core for PCI-Express

### Deliverables

- Encrypted VHDL Source Code for easy Designflow integration
- Comprehensive User Guide
- Reference Design
- Windows / Linux Driver Package (Option)
- PCI-Express Testbench with High Speed simulation mode
- Technical support

### Evaluation

This IP Core can be evaluated as an encrypted version. Request a free evaluation at:

[ip@smartlogic.de](mailto:ip@smartlogic.de)

Smartlogic is a member of  
Xilinx's Alliance Program.



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