SMARTLOGIC
creating smart FPGA/ASIC solutions

Product Brief

August 2018

Multifunction Extension IP Core for Xilinx FPGAs

Product Overview

The PCI Express Specification allows Endpoints that incorporate more than one physical PCIe-Function. Such Endpoints are called Multi-Function Devices. The big advantage of a Multi-Function Device is, that a separate device driver can be associated to each physical Function. This simplifies driver development and maintenance significantly by separating different peripheral Functions logically into different device drivers.
The Xilinx PCIe Hardblocks in the 7 Series device family however do not support more than one physical PCIe Function and do not support Multi-Function Devices natively.
Smartlogic's new patented Multi-Function Extension IP-Core removes this restriction by extending the Xilinx PCIe Hardblock with up to 6 physical PCIe Functions. Compared to a PCIe Soft IP-Core solution with Multi-Function support, the Smartlogic IP-Core uses only a fraction of logic resources and will fit even in the smallest Artix FPGA Devices.

IP Core Facts Table				
Core Specifics				
Supported Device Family	Artix-7, Kintex-7, Zynq-7000			
Resources				
Configuration	PCIe-Functions	FPGA-Resources (1)		
Width / Speed		LUTs	FFs	BRAM
X1, Gen 2	2	3151	3436	8
X1, Gen 2	4	3548	4038	8
Provided with the Core				
Design Files	Encrypted HDL Source			
Example Design	VHDL			
Simulation Model	Encrypted VHDL			
Driver Package	Linux or Windows Source Code as option			
Tested Designflows				
Design Entry	Vivado Design Suite			
Simulation	Vivado Simulator, ModelSim			
Synthesis	Vivado Synthesis			
Support				
Provided by Smartlogic				

(1) These numbers include the resources of the Xilinx AXI Stream Integrated Block for PCI Express Wrapper

IP-Features

- Extends the Xilinx integrated PCI-Sig compliant PCIe Hardblock by up to 6 true physical PCI Express Functions (not virtual Functions requiring SRIOV capability)
- Each BAR of each Function is mapped to an memory mapped AXI4 Master
- The user defines, if all PCIe-Functions communicate with either the same or with a different device driver
- 32 and 64-Bit BAR support for all Functions
- BARs can be defined independently at compile time.
- Each Function can issue interrupts (MSI / Legacy)
- Detection of Signal Integrity problems on PCIe Link (for productional testing)
- Device Driver Package available as option
- Link Speeds Gen 1 / 2, Link Widths x1 / x2
- Available for A7, K7 and Zynq-7000 (ask for the availability for other FPGA Families)

Limitations

Due to the low logic footprint approach by using the Xilinx PCIe Hardblock, the User has to be aware of some limitations. For most applications these are considered as minor and acceptable.

- The maximum supported number of physical PCIe Functions is 6
- The sum of active BARs of all Functions is limited to 6
- Each function has to use the same interrupt mode (Legacy or MSI) with the same vector amount
- For other minor limitations, see the User Guide

Contact

Smartlogic GmbH
D-71157 Hildrizhausen
Phone: (+49) 7031 - 439016
Fax: (+49) 7031 - 439018
www.smartlogic.de
ip@smartlogic.de

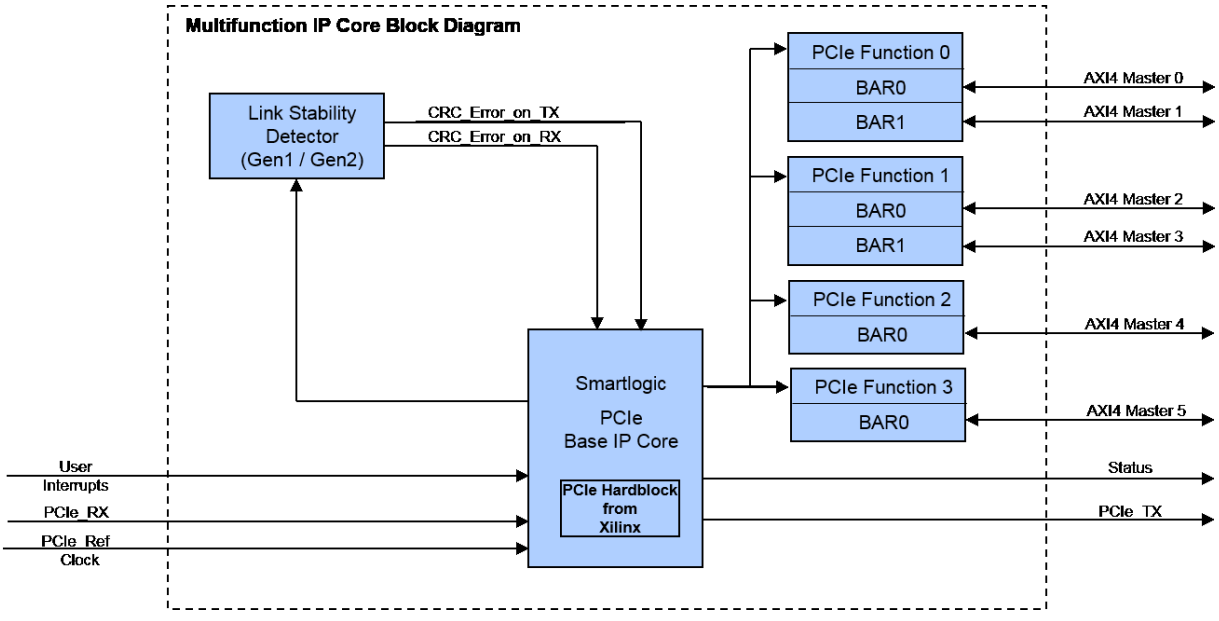
SMARTLOGIC
creating smart FPGA/ASIC solutions

Product Brief

August 2018

Multifunction Extension IP Core for Xilinx

Block Diagram:



The block diagram shows 4 of the 6 available PCIe Functions and an example mapping of the function's BARs.

The User has full control at compile time to map up to 8 AXI Masters to the active PCIe Functions.

Unused AXI4 Masters do not occupy logic resources.

Minimum Speedgrades:

FPGA Device	Link Width / Link Speed	Minimum Speedgrade
Artix	X1 / Gen 1	-1
	X1 / Gen 2	-2
Kintex	X1 / Gen1 or Gen2	-1

For Zynq-7000 Devices, use the Artix or Kintex speedgrades.

Contact

Smartlogic GmbH
D-71157 Hildrizhausen
Phone: (+49) 7031 - 439016
Fax: (+49) 7031 - 439018
www.smartlogic.de
ip@smartlogic.de

SMARTLOGIC
creating smart FPGA/ASIC solutions

Product Brief

August 2018

Multifunction Extension IP Core for Xilinx

Example Configuration with 4 PCIe Functions

The following example shows the PCIe Configuration Space for 4 Functions. The BAR Layout is user defined. In this example, Function 0 contains one 64-Bit BAR, Function 1 two 32-Bit BARs and Function 2 and 3, one 32-Bit BAR.

Config Space FN0	Config Space FN1	Config Space FN2	Config Space FN3
Device / Vendor ID	Device / Vendor ID	Device / Vendor ID	Device / Vendor ID
Status / Command	Status / Command	Status / Command	Status / Command
Classcode / Rev ID N	Classcode / Rev ID N+1	Classcode / Rev ID N+2	Classcode / Rev ID N+3
Bist / Header Type Lat. Timer / Cache Line	Bist / Header Type Lat. Timer / Cache Line	Bist / Header Type Lat. Timer / Cache Line	Bist / Header Type Lat. Timer / Cache Line
BAR 0	BAR 0	BAR 0	BAR 0
BAR 1	BAR 1	BAR 1 (disabled)	BAR 1 (disabled)
BAR 2 (disabled)	BAR 2 (disabled)	BAR 2 (disabled)	BAR 2 (disabled)
BAR 3 (disabled)	BAR 3 (disabled)	BAR 3 (disabled)	BAR 3 (disabled)
BAR 4 (disabled)	BAR 4 (disabled)	BAR 4 (disabled)	BAR 4 (disabled)
BAR 5 (disabled)	BAR 5 (disabled)	BAR 5 (disabled)	BAR 5 (disabled)
Cardbus CIS Pointer	Cardbus CIS Pointer	Cardbus CIS Pointer	Cardbus CIS Pointer
Subsyst ID / Subvendor ID	Subsyst ID / Subvendor ID	Subsyst ID / Subvendor ID	Subsyst ID / Subvendor ID
Expansion ROM Address (disabled)	Expansion ROM Address (disabled)	Expansion ROM Address (disabled)	Expansion ROM Address (disabled)
Cap Pointer	Cap Pointer	Cap Pointer	Cap Pointer
Reserved	Reserved	Reserved	Reserved
Max Lat/Min Gnt/I-Pin/I-Line	Max Lat/Min Gnt/I-Pin/I-Line	Max Lat/Min Gnt/I-Pin/I-Line	Max Lat/Min Gnt/I-Pin/I-Line

In this example the Revision ID Register is configured, that it increments with each Function in order to associate different device drivers for each Function.

Evaluation

This IP Core can be evaluated on Xilinx Demoboards like the AC701. Request a free evaluation at:
ip@smartlogic.de

Partnership

Smartlogic is a member of Xilinx's Alliance Program since 2006.

XILINX
| ALLIANCE PROGRAM

Contact

Smartlogic GmbH
D-71157 Hildrizhausen

Phone: (+49) 7031 - 439016
Fax: (+49) 7031 - 439018

www.smartlogic.de

ip@smartlogic.de