SMARTLOGIC

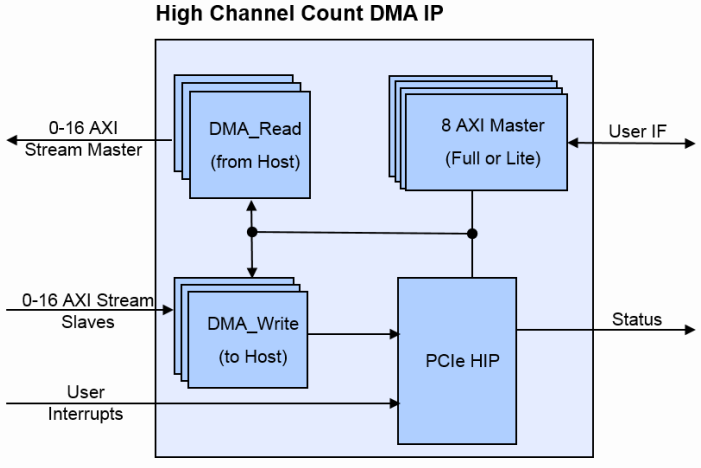
Product Overview

December 2021

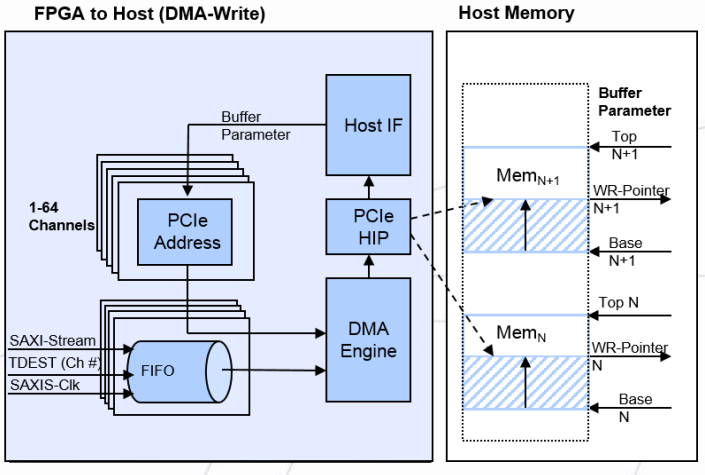
High Channel Count DMA IP Core for PCI-Express

Product Overview

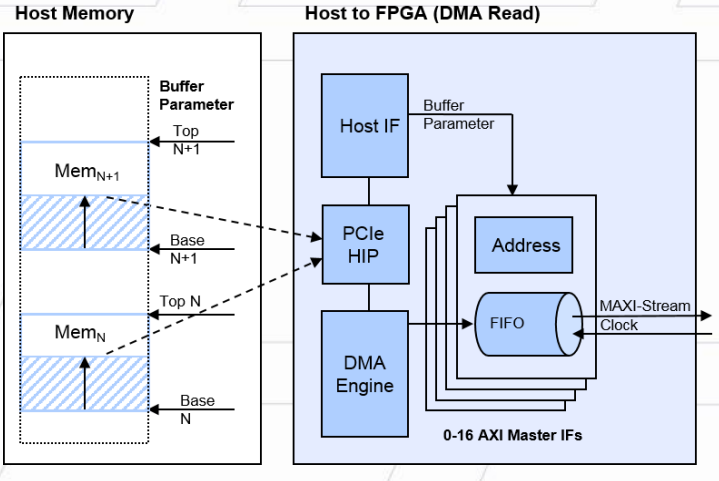
The High Channel Count (HCC) DMA IP core for PCI-Express is a powerful PCIe Endpoint with multiple industry standard AXI Interfaces. This IP addresses continuous streaming applications from up to 64 different data sources. Each channel is able to transmit data into a separate memory area. Up to 16 AXI Stream masters read DMA Data from the host and present it to the user logic. Additional 8 AXI4 masters are available to interface full AXI or AXI-Lite peripherals with the host.
The link stability detector module measures the signal integrity of the PCI Express Link for lab or production tests to prevent shipments of faulty devices (Xilinx only).
This IP core enables the developer to build complex PCI Express endpoints with no specific PCI Express protocol know how. The user only transmits or receives payload data and does not have to assemble valid PCI Express packets.



Block Diagram of the IP Core (simplified)



DMA Write Details



DMA Read Details

IP-Features

- Available for Xilinx or Intel FPGAs
- User transmits / receives only user data without PCIe protocol knowledge
- AXI standard interfaces for easy integration
- All AXI interfaces have adjustable data width and separate clocking
- Supports up to 64 independent host buffers
- adjustable priority control
- Supports memory with adjustable pagesize
- Supports linear contiguous memory as ringbuffers
- Memory Size up to 4 GByte per streaming channel
- Performance only limited by PCI Express bandwidth
- Based on Xilinx / Intel integrated PCI-Sig compliant PCIe Block (HIP)
- Link Speeds Gen1-3, Link Widths x1-x8
- Multifunction supported as an option

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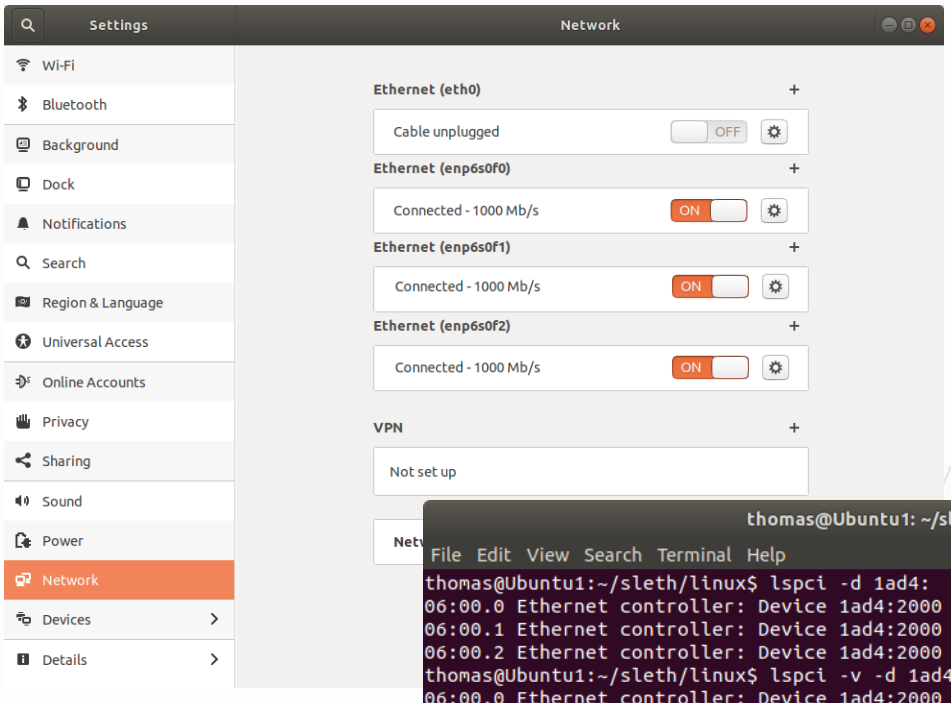
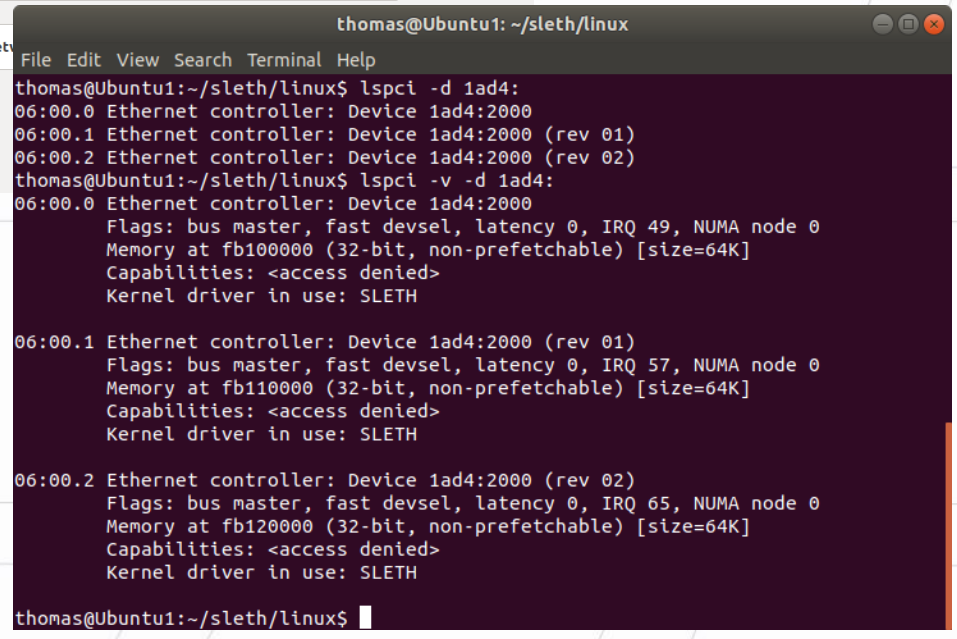
IP Application “Ethernet”

The HCC IP core allows to add additional ethernet links to the host via PCI Express. Ethernet link speed is at your choice and limited by the PCIe bandwidth. The Smartlogic device driver integrates these new links into Linux in order to allow access to the user.

In conjunction with the PCIe multi-function option it is possible to connect up to 8 ethernet links that share the same PCIe connection to the FPGA. The exact number of ethernet links depends on the multi-function capabilities of the PCIe HardIP block of the FPGA. Check with your FPGA vendor if multi-function is supported and how many physical functions are available for PCI Express.

This example shows 3 additional ethernet links on a Cyclone 5 device and how they appear on Linux:





A complete reference design is available to demonstrate this use case.

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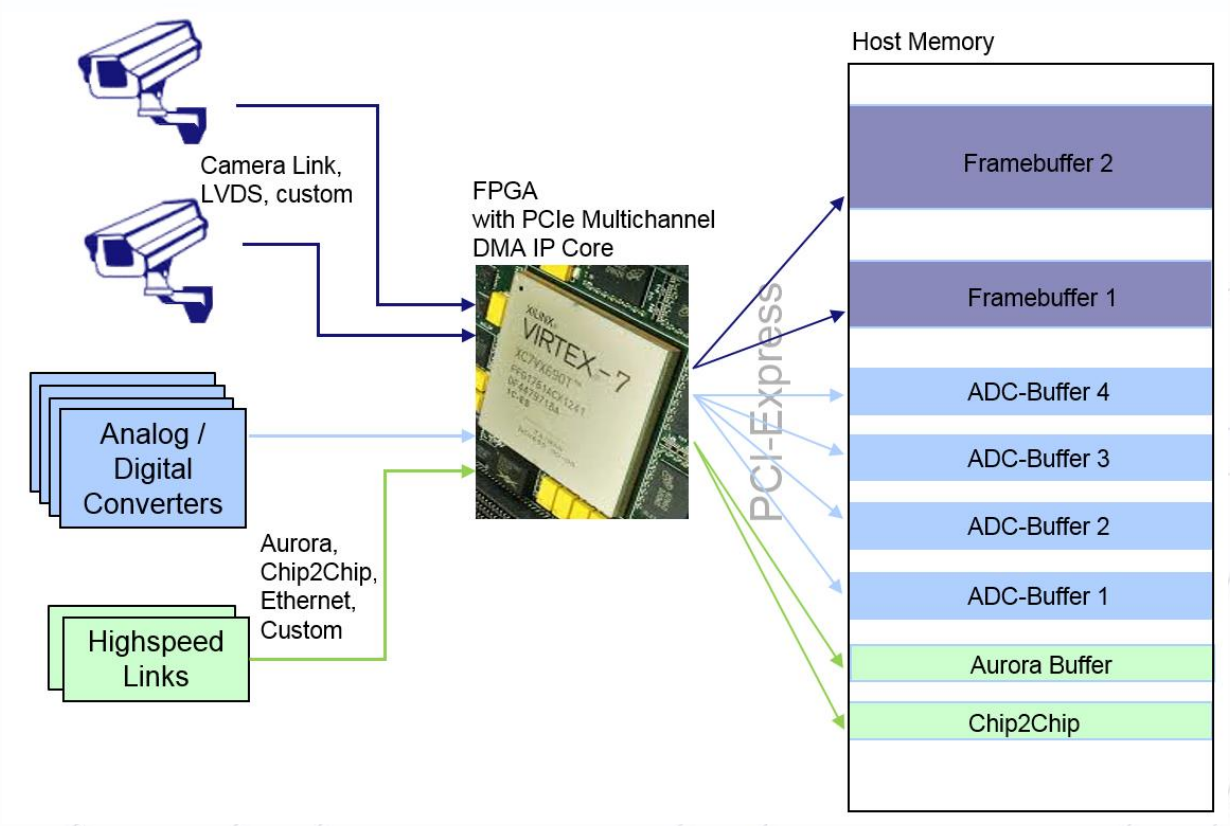
IP Application "Streaming"

Due to its generic architecture, the Multichannel DMA IP Core for PCI Express fits into many applications.
The following diagram shows the typical streaming application, where data streams have to be sent ordered to the host memory:



Typical streaming data sources are :
Video Cameras, Highspeed Analog-Digital-Converter Samples, Highspeed Links like Aurora, Ethernet or others.
Up to 64 independent streaming sources with a dedicated Target Buffer are supported.
Each data interface can operate at its own clock domain and its own data width (8, 16, 32, 64, 128 or 256 Bit).
The target can be either the Host Memory or any other PCI Express endpoint in the system.

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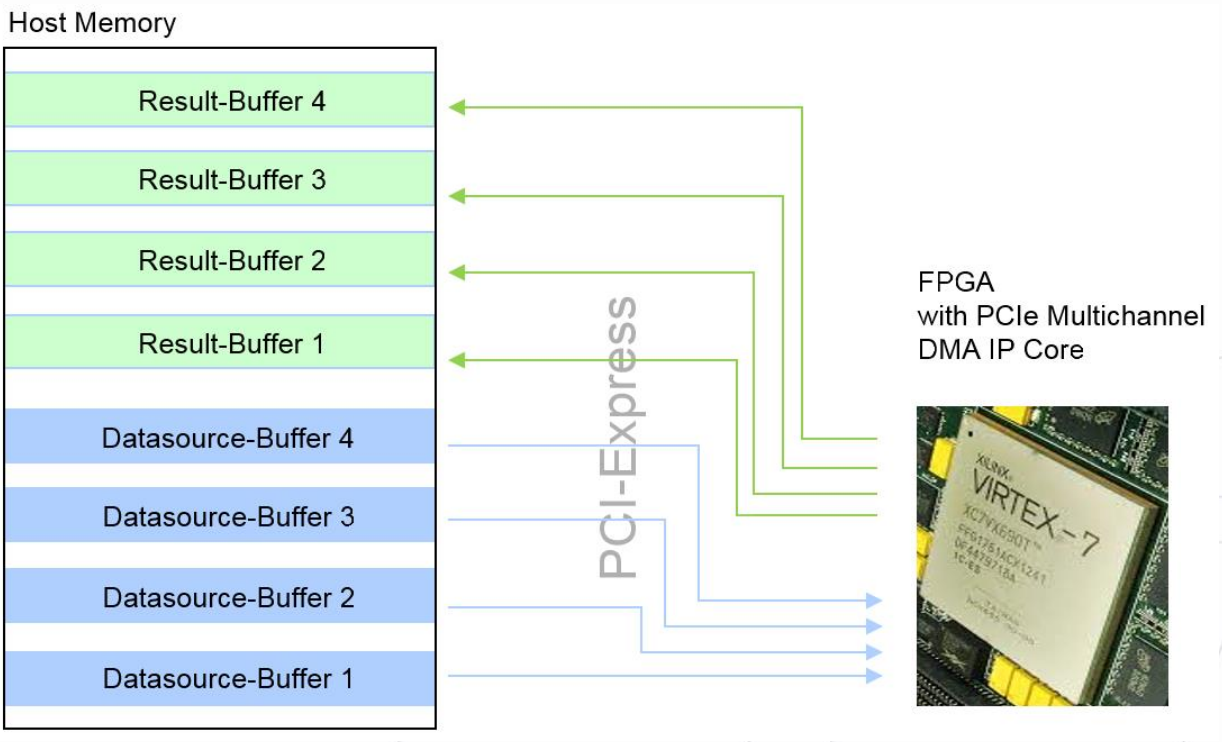
IP Application "Co-Processor"

Another well known application is the custom data Co-Processor within a FPGA. The data which has to be processed is either fetched via DMA Read Requests from the FPGA or served from the CPU or another PCI Express endpoint. The processed results will be written back into separate memory buffers by using DMA Write Requests. Application examples are data encryption and Video Data processing.



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FPGA resource utilization

The following table lists different example configurations and the needed FPGA resources:

FPGA Family	Configuration	FPGA-Resources(1)					
	Width / Speed	LUTs	LUTR(2)	FFs	BRAM	PCIE	Misc
Artix 7 Kintex 7	64 bit Architecture, 32 DMA Write Channels, 1 Master, 0 Read Channels	5,583	235	7,377	9	1	1 MMCM
7 Series, Ultrascale Ultrascale+	256 bit Architecture, 9 DMA Write, 1 Master, 8 Read interfaces	20,845	3,969	27,887	70	1	1 MMCM
		ALMs		FFs	BRAM	PCIE	Misc
Cyclone 5, Arria 5 / 10, Stratix 10	256 bit Architecture, 64 DMA Write Channels, 1 AXI Master, 2 Read Channels	10,373		13,562	81	1	6 PLL
Cyclone 5, Arria 5 / 10, Stratix 10	256 bit Architecture, 9 DMA Write, 1 Master, 8 Read interfaces	18,204	3,510	25,077	129	1	6 PLL

(1) These numbers include the resources of the PCIe Hard-IP and the resources for the AXI Stream FIFOs for each configured channel.

(2) LUTR are distributed RAM Cells. The user can choose between BlockRAM or LUT RAM Implementation style.

Deliverables

- Encrypted VHDL or Source Code for easy designflow integration
- Comprehensive user guide and app notes
- Reference design
- Windows / Linux driver package (option)
- PCI-Express testbench with high speed simulation mode
- Technical support

Evaluation

This IP Core can be evaluated as an encrypted version. Request a free evaluation at:

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Smartlogic is a member of Xilinx's Alliance Program.

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