SMARTLOGIC
smart PCI Express solutions

Product Brief

January 2021

PCI Express Multifunction IP Core for Intel Cyclone V / Arria V FPGAs

Product Overview

The PCI Express specification allows endpoints that incorporate more than one physical PCIe function. Such endpoints are called multifunction devices. The big advantage of a multifunction device is, that a separate device driver can be associated to each physical function. This simplifies driver development and maintenance significantly by separating the peripheral functions logically into different device drivers.

The Intel PCIe hardblocks in the Cyclone V / Arria V FPGA device families support multi-function devices natively but on a very low level.

Smartlogic's PCI Express multifunction IP core for Cyclone V FPGAs offers a fully productized IP core with optional DMA support. The core operates with industry standard interfaces (AXI and AXI Stream) and encapsulates the whole PCI Express protocol know-how. This frees the FPGA designer to concentrate on the project specific design tasks.

IP Core Facts Table				
Core Specifics				
Supported Device Families	Cyclone V, Arria V			
Resources				
Configuration	PCIe-Functions	FPGA-Resources [1]		
Width / Speed		ALMs	FFs	BRAM
X1, Gen2, 4 AXI Masters	4	2507	4354	2 M10K
Provided with the Core				
Design Files	Encrypted HDL (Source Code as option)			
Example Design	VHDL			
Simulation Model	Encrypted VHDL			
Driver Package	Linux or Windows (Source Code as option)			
Toolchain				
Design Entry	Quartus Prime Lite			
Simulation	ModelSim, Aldec Riviera, Cadence Incisive			
Synthesis	Quartus Prime Synthesis			
Support				
Provided by Smartlogic				

[1] These numbers include the resources of the Intel HIP for PCI Express

IP-Features

- Utilizes the Intel PCIe HIP block with up to 8 physical PCIe functions.
- Designs provides up to 8 AXI masters which can be freely mapped to the PCIe functions
- Optional DMA support (Flex or HCC IP core)
- The user defines, if all PCIe functions communicate with either the same or with a different device driver
- 32 and 64-Bit BAR support for all functions
- BARs can be defined independently at compile time.
- Each function can issue interrupts (MSI Interrupts recommended)
- Device driver package available as option
- Link speeds Gen 1 or 2, Link width x1-x4, (x8 possible with Arria V)
- Available for Cyclone V and Arria V FPGAs (ask for the availability for other FPGA families)

Limitations

For Intel FPGAs, there is one slight limitation for this IP core.

- When issueing interrupts, each function has to use MSI mode with the same amount of interrupt messages

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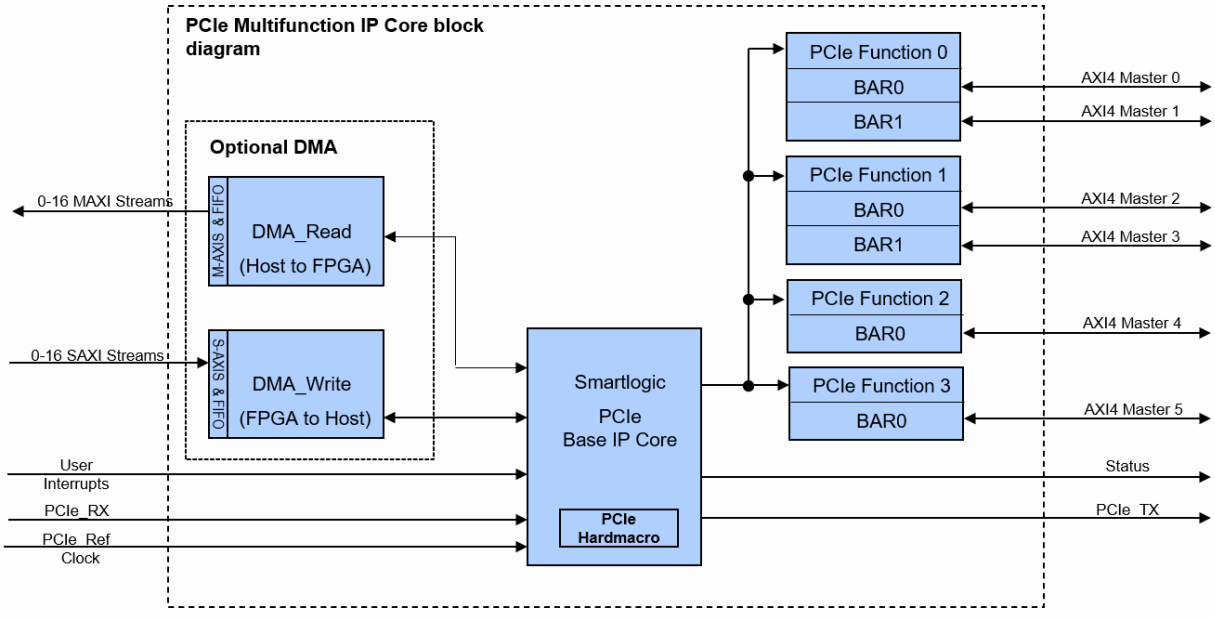
Example configuration:



The example shows 4 of the 8 available PCIe functions and how the BARs of each function can be mapped to AXI masters. The User has full control at compile time to map up to 8 AXI masters to the active PCIe functions. Unused AXI4 masters do not occupy logic resources.

Minimum Speedgrades:

FPGA Device	Minimum Speedgrade	Comment
Cyclone V	-7	Check for further Intel specific speedgrade requirements when using the Core at Gen2 rates
Arria V	-6	

Evaluation

This IP core can be evaluated on Intel demoboards like the Cyclone V GX Development Kit. Request a free evaluation at:

ip@smartlogic.de

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